NMOS Digital Circuits

Introduction
Static NMOS circuits
Dynamic NMOS circuits
Introduction

• PMOS and NMOS families are based on MOS transistors with induced channel of \( p \) respectively \( n \)
• NMOS circuits mostly used for switching (higher speed)
• Circuits are using exclusively NMOS transistors
• One positive power supply
• Logic levels are function of power supply voltage level
Transistor $T_1$ acts as an inverter
$T_2$ acts as active load, replacing the static resistor
MOS technology uses transistors as playing the role of a resistor
$T_1$ is based on n channel, in enhancement mode; $T_2$ works in depletion mode
It means: $T_1$ threshold voltage positive and $T_2$ being negative
External load is normally also NMOS inputs, so there is a huge input resistance
and the load has mainly a capacitance meaning
Transfer Characteristic

Area a, \( V_i < V_{T1} \), T1 is off, \( I_{DS1} = 0 \), \( V_o = V_{DD} \), T2 works in linear regime

Area b, \( V_i > V_{T1} \), T2 works in linear region. \( V_{DS1} > V_{GS1} - V_{T1} \), T1 saturated. For T2 being in linear region, \( 0 \leq V_{DS2} \leq V_{GS2} - V_{T2} \), where \( V_{GS2} = 0 \), and \( V_{DS2} = V_{DD} - V_o \), therefore \( V_o \) must be higher than \( V_{DD} + V_{T2} \), making at input:

\[
V_{T1} < V_i < V_{T1}(1 + \sqrt{2})
\]

Area c

\( V_i = V_{T1}(1 + \sqrt{2}) \)

T2 saturated
T1 saturated for:

\[
\frac{V_{DD}\sqrt{2}}{4} \leq V_o \leq \frac{V_{DD}}{2}
\]

Here transfer characteristic is linear and abrupt

Area d, T1 off saturation and enter linear regime; T1 goes off saturation for:

\[
V_i \approx \frac{V_{DD}^2}{16} \cdot \frac{1}{V_0} + \frac{V_{DD}}{8} + \frac{V_o}{4}
\]
Threshold Voltage

- Function of supply voltage for the basic substrate and the doping index
- Usually the substrate terminal is tied together with the source terminal, in most cases tied to ground
- Sometimes there is a voltage substrate-source, allowing a control (adjustment) of the threshold voltage
Load resistance

Built using a transistor: $T_2$  
Gate connected to $V_{GG}$  
$T_1$ on, for having $V_o$ very close to zero, $R_{T2} \gg R_{T1}$:  
$$\frac{W_1/L_1}{W_2/L_2} >> 1$$  
$R_{T1}$ has values: 0.5 up to 10KΩ  
If $R_{T1}=10KΩ$ then $R_{T2}=250KΩ=R_s$

$$V_o = \frac{V_{DD}}{R_s + R_{T1}} R_{T1}$$

For $V_{DD} = 15V$, $V_o = 0.5V$

If $T_1$ off, $V_o = V_{GG} - V_{T2}$, for $V_o$ being approx. $V_{DD}$, must:

$V_{GG} = V_{DD} + V_T$
Static NAND Gate

T₁ and T₂ connected serially, the logic inputs are applied on their gates circuits

T₃ load resistance

For making ‘better’ output voltage levels, mainly the low level very close to 0V, the active resistance must be much greater (20 times) the passing resistance of the input transistors

Not recommended to serially connect too many input transistors, because the load resistance would become too important and the switching times would grow, damaging the gate’s dynamic behavior

If at both inputs applied $V_{IH} = V_{DD}$, T₁ & T₂ on, $V_o \approx 0V$

If at least, one input has $V_{IL} = 0V$, corresponding transistor(s) goes off and $V_o \approx V_{DD}$

$$F = \overline{AB}$$
Static NOR Gate

T₁ & T₂ connected in parallel, their gates are the input circuits.

T₃ acts as load resistance.

Connecting input transistors in parallel doesn’t affect the load resistance, so the number of circuit inputs isn’t bounded by dynamic considerations.

If both inputs have: $V_{IL} = 0V$, T₁ & T₂ off, $V_o \approx V_{DD}$

If applying at least at one input $V_{IH} = V_{DD}$, that input transistor is on, $V_o \approx 0V$

\[ F = \overline{A + B} \]
Implementing logic function

Using the serial and parallel MOS transistors connections, complex logic functions may be implemented, with a simple structure of the integrated circuit; see behind.
Static AND, OR & XOR Gates

AND & OR gates are built up by inverting the signal from the output of NAND, respectively NOR gates, using an extra inverter, made with transistors T₄-T₅.

For XOR gate: Vₒ = “0” for two cases: if T₁ & T₂ are on (A & B inputs both “1”) or if T₅ & T₆ are off (A & B inputs both “0”) (in this case in the gate of T₄ there is a voltage approx. V_DD making the transistor on.)
Dynamic NMOS circuits

- A basic method to store (memorise) the logic values is to use the input capacitances of the MOS transistors.
- A capacitance with no stored charge (discharged) is said to represent a logic ‘0’, respectively a charged capacitance is said to represent a logic "1".
- Signals are applied in the gate circuit, from one capacitor to the other, using transistors driven in conduction by special driving signals (command pulses).
- Operate in a small dissipation power regime.
- Dynamic MOS circuits offer a better integration density than the static ones.
- Transistors performance doesn’t depend on their geometry.
- Drawback: more driving (command) signals, more logic.
Dynamic NMOS Inverter

Inverter built up from transistors Q1 & Q2, together with capacitance C1

Output circuit made from transistor Q3 and storage capacity C2

There are clock signals:

- $V_{p1}$, applied on Q2 gate, sampling input value $V_{in}$, then inverted by Q1 and stored (memorised) by C1
- $V_{p2}$, applied on Q3 gate, making it open and ‘copying’ the stored charge from C1 to C2
Dynamic NMOS Inverter

Example of operation:
t=t₀, \( V_{in} = \text{‘0’} \), apply pulse \( V_{p1} \): \( Q_1 \) off, \( Q_2 \) on and from \( V_{DD} \) charges \( C_1 \)
t=t₁, apply pulse \( V_{p2} \), \( Q_3 \) goes on, charge from \( C_1 \) is transmitted on \( C_2 \)
If \( C_1 \gg C_2 \), transfer of charge is without important losses, and on \( C_2 \) there will be a potential corresponding to logic ‘1’

\[ t_2 < t < t_3, \ V_{in} = \text{‘1’}, \ Q_1 \text{ on, } C_1 \text{ loses charge through } Q_1 \]
t=t₄, pulse \( V_{p2} \), \( Q_3 \) open, \( C_1 \) without charge, so will become \( C_2 \), so output logic “0”

For this inverter, the output response is delayed with \( t_1 - t_0 \) or \( t_4 - t_2 \)
Pulses \( V_p \) need to be applied periodically, achieving the refresh of the information stored on parasitic capacitances
A minimum refresh frequency must be designed, to keep right information on capacitances, which otherwise discharge through existing open junctions
Low-power dynamic NMOS inverter

- Input circuit built using $Q_1$ și $C_1$, transistor driven by $V_{p1}$
- A $V_{p1}$ pulse makes input transfer on $C_1$ and in the same time keeps capacitance $C_2$ at a potential equivalent with the inverted input information
- Input circuit consumes from power supply only on $V_{p1}$ driving signal for input transistor
NAND & NOR Dynamic NMOS gates

- Logic function implemented similar way as of the static gates
- Operation is similar with that described for dynamic inverter
Dynamic AND-OR-NOT Gate

Circuit operates synchronously, gate response triggered at output by pulse $V_{p2}$
For pulse $V_{p1}$, logic levels from A, B, and C inputs are stored on capacitances from the gates of transistors $T_5$, $T_4$, $T_6$ (which mean the basic gate structure)

Transistors with logic '1' inputs will be on, and those with logic '0' will be off
Pulse $V_{p2}$, makes $T_7$ open (gate’s load active resistance)
Output Y depends on the global state of transistors $T_4$, $T_5$, $T_6$

$Y = '0'$ if $T_6$ is on, or $T_4$ and $T_5$ are both on

$Y = A \cdot B + C$