CONVERTERS

Filters
Introduction to Digitization
Digital-to-Analog Converters
Analog-to-Digital Converters
Filters

Filters are used to remove *unwanted* bandwidths from a signal. Filter classification according to implementation:

**Active filters** include RC networks and op-amps. Suitable for low frequency, small signal. Active filters are preferred since they avoid the bulk and non-linearity of inductors and can have gains greater than 0dB. However, active filters require a power supply.

**Passive filters** consist of RCL networks. Simple, more suitable for frequencies above audio range, where active filters are limited by the op-amp bandwidth.

**Digital filters**

A digital filter uses a digital processor to perform numerical calculations on sampled values of the signal. The processor may be a general-purpose computer such as a PC, or a specialized DSP (Digital Signal Processor) chip.
Filter classification according to frequency response
Low-pass filter
High-pass filter
Band-pass filter
Band-stop (Notch)
Sampling

Basic process of **sampling** is the gating of an analogue signal by a periodic pulse which will only allow the signal through whilst each pulse is on. The gating signal or the sampling function \( s(t) \) has pulses of constant height, length (\( \tau \)) and separation time (\( T \)).

The analog baseband signal \( v_m(t) \) is usually level shifted, so no part of it is negative; therefore all samples will be positive. See next slide

Multiplying the baseband signal \( v_m(t) \) by the sampling signal \( s(t) \), the sampled signal \( v_s \) is obtained, made from slices (samples). \( v_s = v_m s(t) \)

\( T \ (T_s) \) is the sampling interval, \( f_s = 1/T_s \) is the sampling frequency and \( \tau \) is the sampling time.

The sampling function \( s(t) \) is a train of narrow pulses; by Fourier analysis, the associated spectrum has the form of a series of harmonics of the pulse repetition frequency \( f_s \), with a sinc envelope having zeros at harmonics of \( 1/\tau \) -- see following slides

Because usually \( \tau \ll T \), a simplification can be made for the first harmonics -- \( \text{sinc}(n\pi \tau/T) \sim 1 \), giving a spectrum with constant amplitude.
Action of sampling
Spectrum of the sampling function

Simplified spectrum of the sampling function for $\tau \ll T$

$T = 5\tau$

$T \gg \tau$
The result of sampling is the function:

\[ v_s = v_m s(t) = (A_m \tau/T)[1 + \cos\omega_m t + \cos(\omega_s-\omega_m)t + 2\cos\omega_s t + \cos(\omega_s+\omega_m)t + \cos(2\omega_s-\omega_m)t + 2\cos2\omega_s t + \cos(\omega_s+\omega_m)t + \ldots] \]

The spectrum is given by the next slide.

To recover the original baseband by filtering, the **Nyquist criterion** must be met. The sampling rate must be at least twice the highest baseband frequency:

\[ f_s \geq 2 f_m (= f_N), \] where \( f_N \) is said to be Nyquist frequency.

Practically, if the sampling occurs at too slow a rate, the lower sideband \((f_s - f_m)\) of the sampling frequency overlaps the baseband, corrupting it. Nyquist criterion is illustrated by the figure next slide.

Another problem avoided using this criterion is **aliasing**; a lower sideband of \( f_s \) can appear within the baseband range and be thought to be part of it (disguised itself, taking a false name – alias). See next slides

It happens when the original signal is affected by noise (presents higher frequency than highest signal frequency); use of low-pass filter or anti-aliasing filter.
Spectrum of sampled signal

Nyquist criterion
Quantization

Quantization is an interpretation of a continuous quantity by a finite set of discrete values; means establishing numerical (binary) values, starting from an analog signal value

Using N bits, may obtain $2^N$ levels; each value of each sample will have associated a N bit binary value

Amplitude quantization approximates its input by a discrete amplitude taken from finite set of values

Quantization step size will be done by:

$$Q_s = \frac{V_{\text{max}} - V_{\text{min}}}{2^N - 1}$$

Quantization error means the difference between the signal’s value and the associated binary value. (see next figure)
Quantization Error
Sample and Hold

To convert analog signals to digital ones is needed to keep sample’s height until the next sample occurs – sample and hold S/H
Result is a stepped waveform as in figure.
An example of S/H circuit is given below; the role of the capacitor is to be charged quickly (sampling time) and then to hold the sampled voltage until the next sample has to replace it.

Input buffer (amplifier) offers a high input impedance to the analog signal and a low output impedance for a fast charge of the capacitor C.

The output buffer has a high input impedance, denying the hold capacitor to discharge, so having a constant value at its input.
Quantized Sampling

**Theoretical background:** Nyquist sampling theorem: sample at twice the highest signal frequency (for a voice carrying signal with bandwidth of 4kHz, sample at 8kHz, or every 125µsec, having 8000 samples/sec)

**Pulse Code Modulation** *(PCM)*, with the following steps:

- Signal sampling, using the proper sampling frequency (higher than twice the highest signal frequency); samples represented as PAM *(Pulse Amplitude Modulation)* pulses

- Quantification of the samples, using the available number of digits, obtaining the PCM pulses and their digital values; more digits, more accuracy, greater cost

- Digital values representation as pulse trains

**Delta Modulation** – approximates the analogue signal by a staircase function moving up/down by one quantization level at each sampling interval; output function has a binary behavior (moves up or down at each sample interval); method less used in computer networks
Pulse Code Modulation

![Diagram showing pulse code modulation waveform](image.png)

<table>
<thead>
<tr>
<th>Digit</th>
<th>Binary equivalent</th>
<th>Pulse-code waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>0011</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>0100</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0101</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>0110</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>0111</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>1001</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>1010</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>1011</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>1100</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>1101</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>1110</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>1111</td>
<td></td>
</tr>
</tbody>
</table>
Delta Modulation
Converters
Analog to Digital Converters (ADC)

Analog to Digital Converter is transforming an analog input signal into a digital output signal one, quantified using a number of bits, at regular sampling periods. Any ADC contains an analog input and a digital (binary) output.

ADC features:
- AD Conversion takes longer than DAC
- ADC may contain a DAC
- Conversion is timed by a clock signal
- ADC control unit is responsible for conversion, signal generation and data storage

ADC resolution (quantum) given by the lowest input variation giving a code (output) change (dependent upon the number of bits the ADC uses).

ADC presents an inherent quantification error, but also: offset, gain, linearity (integral and differential), hysteresis and monotony errors.
The transfer characteristic is ladder shaped (see it for a 3-bit ADC)

LSB or least significant bit is defined as the minimum increment of the voltage that a
ADC can convert; LSB varies with the operating input voltage range of the ADC

FS stands for full scale where the input may vary

If FS of the input signal is 10V than the LSB

for a 3-bit ADC corresponds to $10/2^3=1.25V$. That is not very good!

However, for a 12 bit ADC the least significant bit will be $10/2^{12}=10/4096=2.44mV$

Main ADC types are:
  - Single slope or ramp (use integration)
  - Successive approximation
  - Dual slope
  - Parallel or ‘flash’
Single slope (ramp) ADC

Composed of three basic elements:
A binary counter
A digital-to-analog converter
An analog comparator

Operation
  Counter is reset
  Analog input is sampled
  While $V_A > V_B$ counter increments
  When $V_A = V_B$ counter stops
and binary code is available at the output

Characteristics
  Relatively slow since conversion time
could be up to $2^N$, where $N$ is the
resolution of the ADC
**Successive approximation ADC**

Basic elements it contains:
- A digital-to-analog converter
- An analog comparator
- A control logic module
- A successive approx. register

Operation is based on a binary search
- Initially, the register provides an output corresponding to half the range (1000…0)
- If the analog input is greater, then MSB=1, else MSB=0

The register performs the same operation from MSB to LSB

Characteristics
- Conversion requires only N steps, where N is the resolution of the ADC
- Conversion times of µs are typical
Successive approximation ADC
Dual slope ADC

Basic elements
- An integrator
- A zero-crossing detector
- A binary counter
- Logic gates and switches

Operation
- Counter is reset and switch is connected to the analog input
- The integrator generates a negative ramp whose slope is proportional to the analog input
  - The comparator goes HIGH, enabling clock pulses into the counter
  - When counter overflows, it resets to zero and the control circuit switches the switch to a reference negative voltage
    - This causes the integrator to generate a positive slope ramp
    - When this ramp reaches zero, the comparator goes low and stops the counter, whose value represents the analog input

Characteristics
- Very high resolution, but also slower (30 conversions/sec)
- Widely used in digital multi-meters
- Insensitive to clock drift, RC drifts and high-frequency noise
Dual slope ADC
Parallel (flash) ADC

Basic elements
- A multiple voltage divider
- A set of comparators
- A priority encoder

Operation
- Analog input applied to all comparators
- Priority encoder converts comparator pattern into binary

E.g.: A 3-bit ADC (see table behind):
- For comparator outputs of 0001111, priority encoder generates 100
- For comparator outputs of 0111111, priority encoder generates 110

Characteristics
- Very fast (e.g., 8-bit ADCs capable of 20 million conversions/sec)
- Very expensive for large N since the number of comparators is 2N-1

<table>
<thead>
<tr>
<th>VA</th>
<th>C7</th>
<th>C6</th>
<th>C5</th>
<th>C4</th>
<th>C3</th>
<th>C2</th>
<th>C1</th>
<th>CBA</th>
</tr>
</thead>
<tbody>
<tr>
<td>VA&lt;1V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>000</td>
</tr>
<tr>
<td>1&lt;VA&lt;2V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>001</td>
</tr>
<tr>
<td>2&lt;VA&lt;3V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>010</td>
</tr>
<tr>
<td>3&lt;VA&lt;4V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>011</td>
</tr>
<tr>
<td>4&lt;VA&lt;5V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>5&lt;VA&lt;6V</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>101</td>
</tr>
<tr>
<td>6&lt;VA&lt;7V</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>110</td>
</tr>
<tr>
<td>VA&gt;7V</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>111</td>
</tr>
</tbody>
</table>
Parallel (flash) ADC
ADC – Final Remarks

ADC resolution equal with the resolution of DAC used (ADC with integration)
Accuracy similar with DAC
Conversion time given by the number of digits; for N bits, a number of $2^N-1$ clock periods
Generally ADC are slow
Use in (measurement) instrumentation (voltmeters)
Digital to Analog Converter (DAC)
A DAC can generate an analog output from a digital input.
DAC's performance is limited by the number of samples it can process and the number of bits that is used in converting the digital code into an analog signal.
The output voltage is a sum of voltage components each one twice another:

\[ V_{out} = U_{ref} \left( \frac{b_1}{2} + \frac{b_2}{4} + \ldots + \frac{b_n}{2^n} \right) \]

Main types of DACs:
- Binary weighted ladder
- R-2R ladder
- Pulse width modulation
Binary weighted ladder DAC

Based on the summing op-amp circuit
  Each input resistor is twice the value of the previous one
  Inputs are weighted according to their resistors
Characteristics
The lowest value resistor R affects the MSB and must have the highest precision
This circuit is impractical for large N since it would require high precision resistors for a wide range

\[ V_o = -(V_R + 0.5V_{2R} + 0.25V_{4R} + 0.125V_{8R} + \ldots) \]
R-2R ladder

Resistors with similar values, so better for integration

Operation
When bit \( k \) is 1, the corresponding switch is connected to \( V_{\text{REF}} \)
When bit \( k \) is 0, the corresponding switch is connected to \( \text{GND} \)
Assume all the legs but one are grounded
The one connected to \( V_{\text{REF}} \) will generate a current that flows towards the inverting input of the op-amp
This current is halved by the resistor network at each node
Therefore, the current contribution of each input is weighted by its position in the binary number

![R-2R ladder diagram](attachment:image.png)
The R-2R operation is better understood by redrawing the resistor network.
In (b) only the MSB is ON.
In (c) only the next bit to the MSB is ON.
Problems:

• An analog signal with a maximum frequency of 20kHz is digitally converted. What is the minimum sampling frequency to be used?

• An ADC system on 8 bits treats an analog signal with the $V_{\text{min}}=0\text{V}$ and $V_{\text{max}}=10\text{V}$. Calculate the quantization step.

\[
Q_s = \frac{V_{\text{max}} - V_{\text{min}}}{2^N - 1} = \frac{10\text{V} - 0\text{V}}{2^8 - 1} = \frac{10}{255} \approx 0.039
\]